Abstract

Multilevel voltage source inverters have been receiving more and more attention from the industry and academia as a choice for high voltage and high power applications. The high voltage multilevel inverters can be constructed with existing low voltage semiconductor switches, which already have a mature technology for handling low voltages, thus improving the reliability of the overall inverter system. These multilevel inverters generate the output voltage in the form of multi-stepped waveform with smaller amplitude. This will result in less dv/dt at the motor inputs and electromagnetic interference (EMI) caused by switching is considerably less. Because of the multi-stepped waveform, the instantaneous error in the output voltage will be always less compared to the conventional two-level inverter output voltage. It will reduce the unwanted harmonic content in the output voltage, which will enable to switch the inverter at lower frequencies.

Many interesting multi level inverter topologies are proposed by various research groups across the world from industry and academic institutions. But apart from the conventional 3-level NPC and H-bridge topology, others are not yet highly preferred for general high power drives applications. In this respect, two different five-level inverter topologies and one three-level inverter topology for high power induction motor drive applications are proposed in this work.

Existing knowledge from published literature shows that, the three-level voltage space vector diagram can be generated for an open-end winding induction motor by feeding the motor phase windings with two two-level inverters from both sides. In such a configuration, each inverter is capable of assuming 8 switching states independent of the other. Therefore a total of 64 switching combinations are possible, whereas the conventional NPC inverter have 27 possible switching combinations. The main drawback for this configuration is that, it requires a harmonic filter or isolated voltage source to suppress the common mode currents through the motor phase winding. In general, the harmonic filters are not desirable because, it is expensive and bulky in nature. Some topologies have been presented, in the past, to suppress the common mode voltage on the motor phase windings when the both inverters are fed with a single voltage source. But these schemes under utilize the dc-link voltage or use the extra power circuit.

The scheme presented in chapter-3 eliminates the requirement of harmonic filter or isolated voltage source to block the common mode current in the motor phase windings. Both the two-level inverters, in this scheme, are fed with the same voltage source with a magnitude of $V_{dc}/2$ where V_{dc} is the voltage magnitude requires for the NPC three-level inverter. In this scheme, the identical voltage profile winding coils (pole pair winding coils), in the four pole induction motor, are disconnected electrically and reconnected in two star groups. The isolated neutrals, provided by the two star groups, will not allow the triplen currents to flow in the motor phase windings. To apply identical fundamental voltage on disconnected pole pair winding, decoupled space vector PWM is used. This PWM technique eliminates the first center band harmonics thereby it will allow the inverters to operate at lower

switching frequency. This scheme doesn't require any additional power circuit to block the triplen currents and also it will not underutilize the dc-bus voltage.

A five-level inverter topology for four pole induction motor is presented in chapter-3. In this topology, the disconnected pole pair winding coils are effectively utilized to generate a five-level voltage space vector diagram for a four pole induction motor. The disconnected pole pair winding coils are fed from both sides with conventional two-level inverters. Thereby the problems like capacitor voltage balancing issues are completely eliminated. Three isolated voltage sources, with a voltage magnitude of $V_{dc}/4$, are used to block the triplen current in the motor phase windings. This scheme is also capable of generating 61 space vector locations similar to conventional NPC five-level inverter. However, this scheme has 1000 switching combinations to realize 61 space vector locations whereas the NPC five-level inverter has 125 switching combinations. In case of any switch failure, using the switching state redundancy, the proposed topology can be operated as a three-level inverter in lower modulation index. But this topology requires six additional bi-directional switches with a maximum voltage blocking capacity of $V_{dc}/8$. However, it doesn't require any complicated control algorithm to generate the gating pulses for bi-directional switches.

The above presented two schemes don't require any special design modification for the induction machine. Although the schemes are presented for four pole induction motor, this technique can be easily extend to the induction motor with more than four poles and thereby the number of voltage levels on the phase winding can be further increased.

An alternate five-level inverter topology for an open-end winding induction motor is presented in chapter-4. This topology doesn't require to disconnect the pole pair winding coils like in the previous propositions. The open-end winding induction motor is fed from one end with a two-level inverter in series with a capacitor fed H-bridge cell, while the other end is connected to a conventional two-level inverter to get a five voltage levels on the motor phase windings. This scheme is also capable of generating a voltage space vector diagram identical to that of a conventional five-level inverter. A total of 2744 switching combinations are possible to generate the 61 space vector locations. With such huge number switching state redundancies, it is possible to balance the H-bridge capacitor voltage for full modulation range. In addition to that, the proposed topology eliminates eighteen clamping diode having different voltage ratings compared to the NPC inverter. The proposed topology can be operated as a three-level inverter for full modulation range, in case of any switch failure in the capacitor fed H-bridge cell.

All the proposed topologies are experimentally verified on a 5 h.p. four pole induction motor using V/f control. The PWM signals for the inverters are generated using the TMS320F2812 and GAL22V10B/SPARTAN XC3S200 FPGA platforms. Though the proposed inverter topologies are suggested for high-voltage and high-power industrial IM drive applications, due to laboratory constraints the experimental results are taken on the 5h.p prototypes. But all the proposed schemes are general in nature and can be easily implemented for high-voltage high-power drive applications with appropriate device ratings.